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(54) **DISPLAY DEVICE**

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(71) Applicant: **Japan Display Inc.**, Tokyo (JP)

(72) Inventor: **Keiichi SAITO**, Tokyo (JP)

(57) **ABSTRACT**

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A display device includes an electroluminescent panel including first light-emitting elements to emit red (first color), second light-emitting elements to emit green (second color), and third light-emitting elements to emit blue (third color); an image analyzer that obtains, in displaying of a received video signal, first power serving as a total of power required for displaying red (first color), power required for displaying green (second color), and power required for displaying blue (third color), and that calculates second power by multiplying the first power by a predetermined coefficient according to the video signal, and calculates threshold power by multiplying, by the coefficient, maximum allowable power that is allowed when the electroluminescent panel performs image display; and a luminance adjuster that multiplies the video signal by a ratio between the threshold power and the second power when the second power is equal to or greater than the threshold power.

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(52) **U.S. Cl.**

CPC **G09G 3/2003** (2013.01); **G09G 3/3266** (2013.01); **G09G 2320/0242** (2013.01); **G09G**

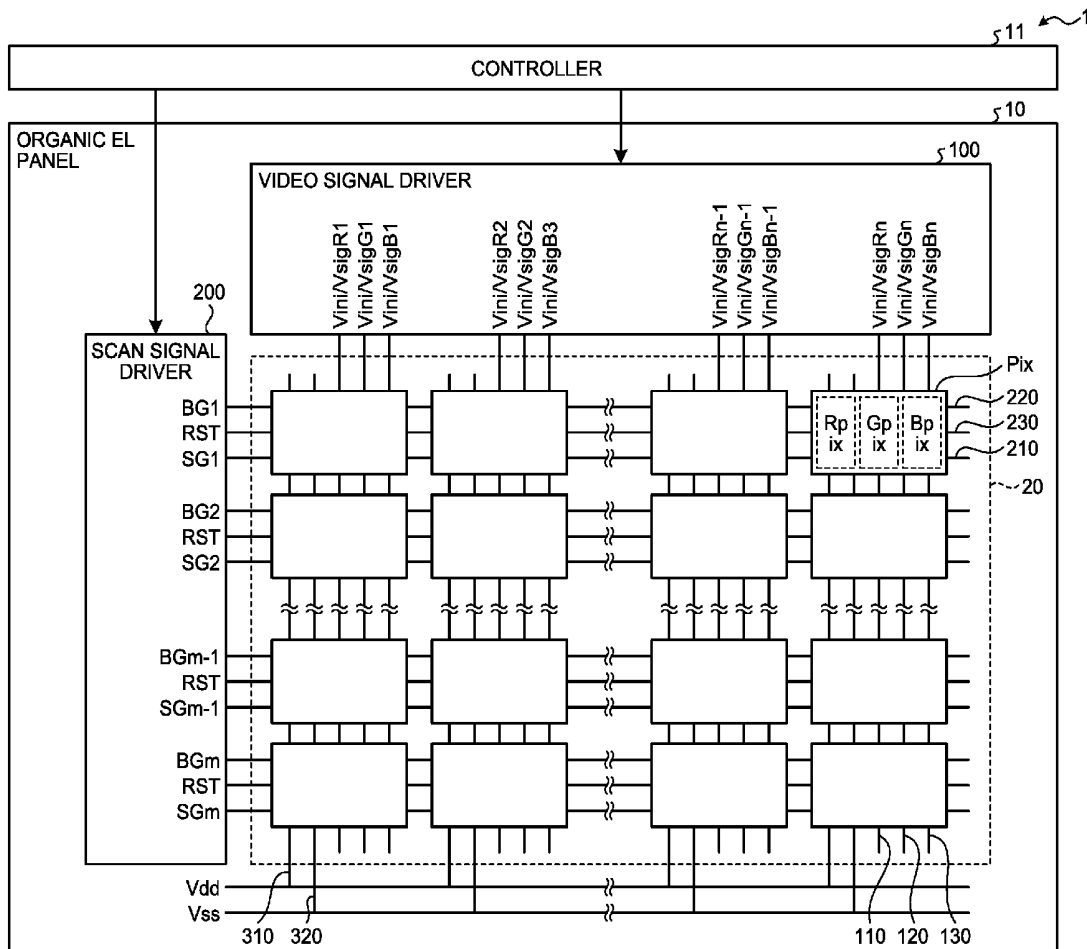
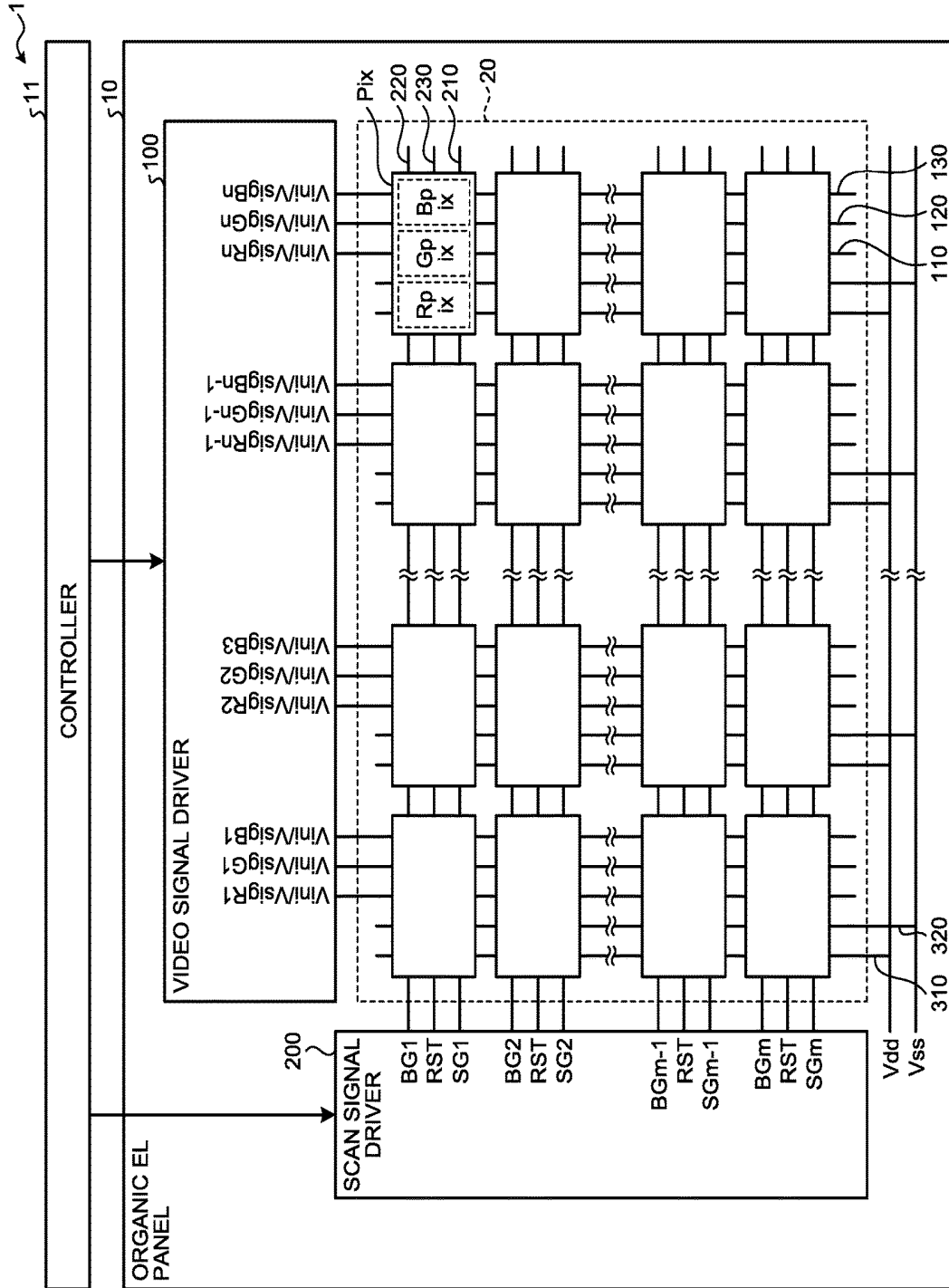


FIG. 1



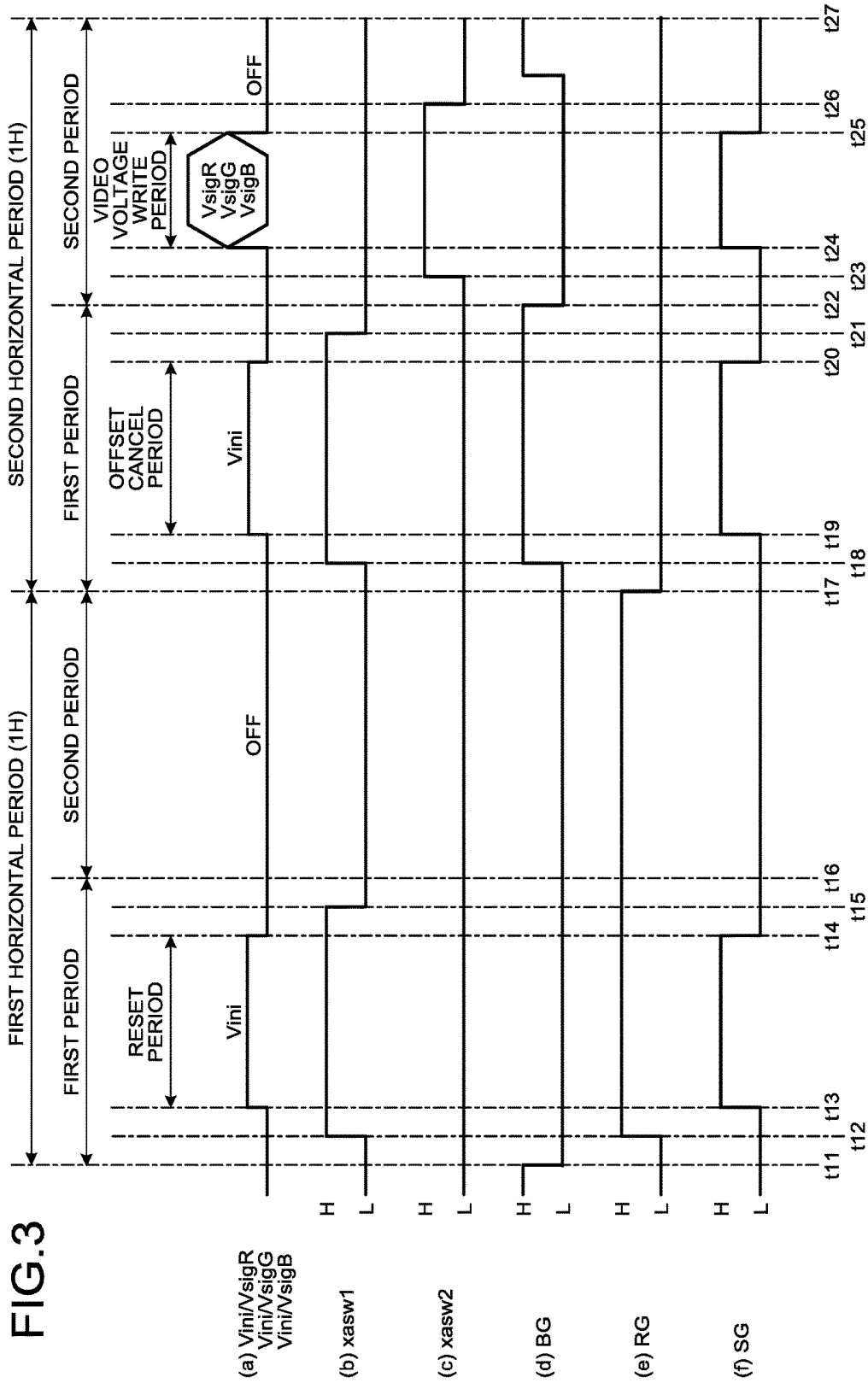


FIG.4

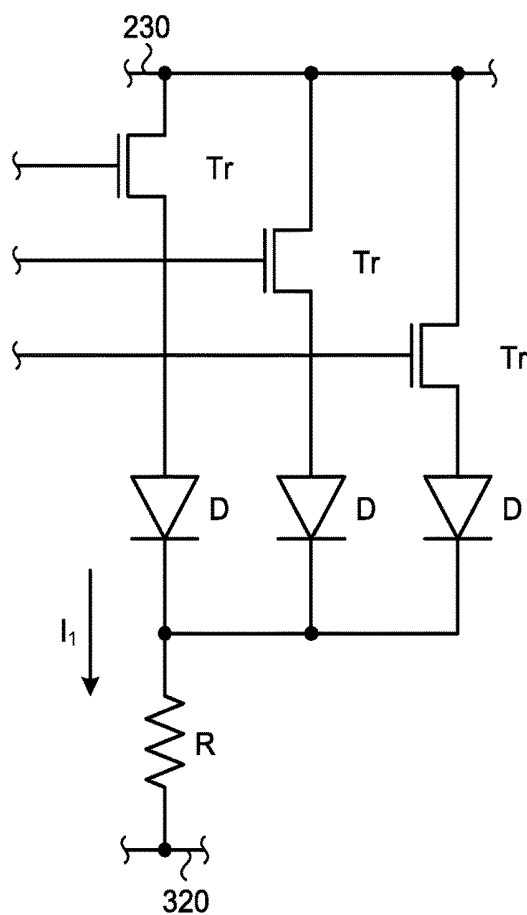


FIG.5

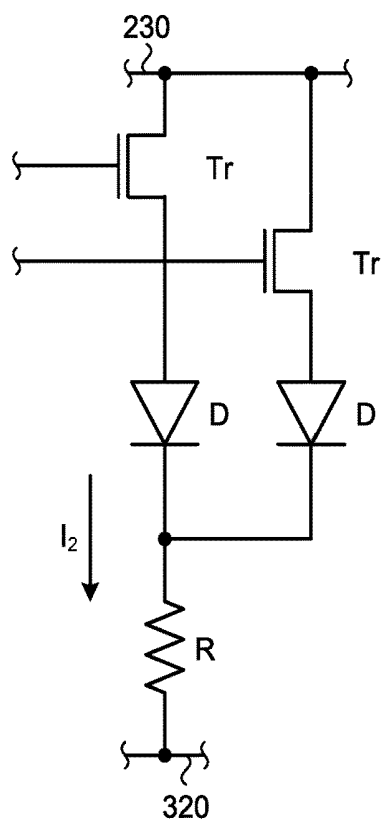


FIG.6

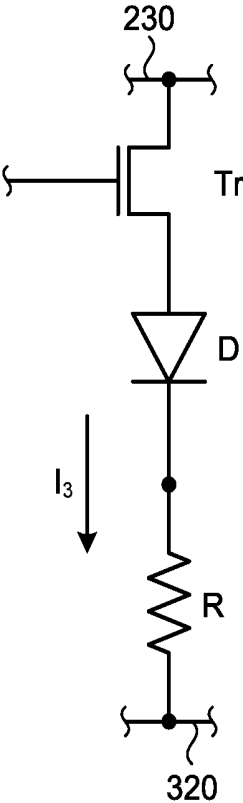


FIG. 7

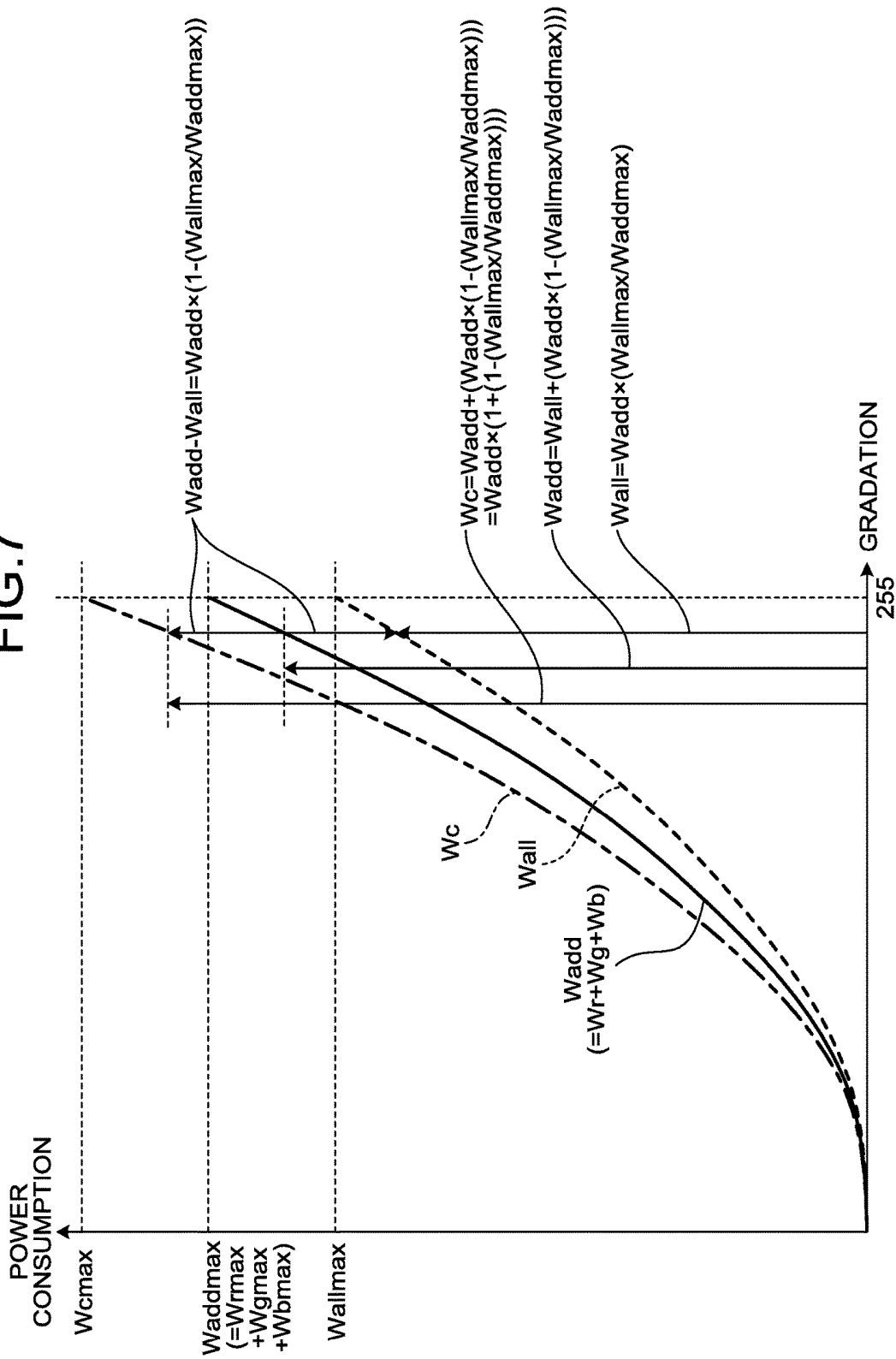


FIG.8

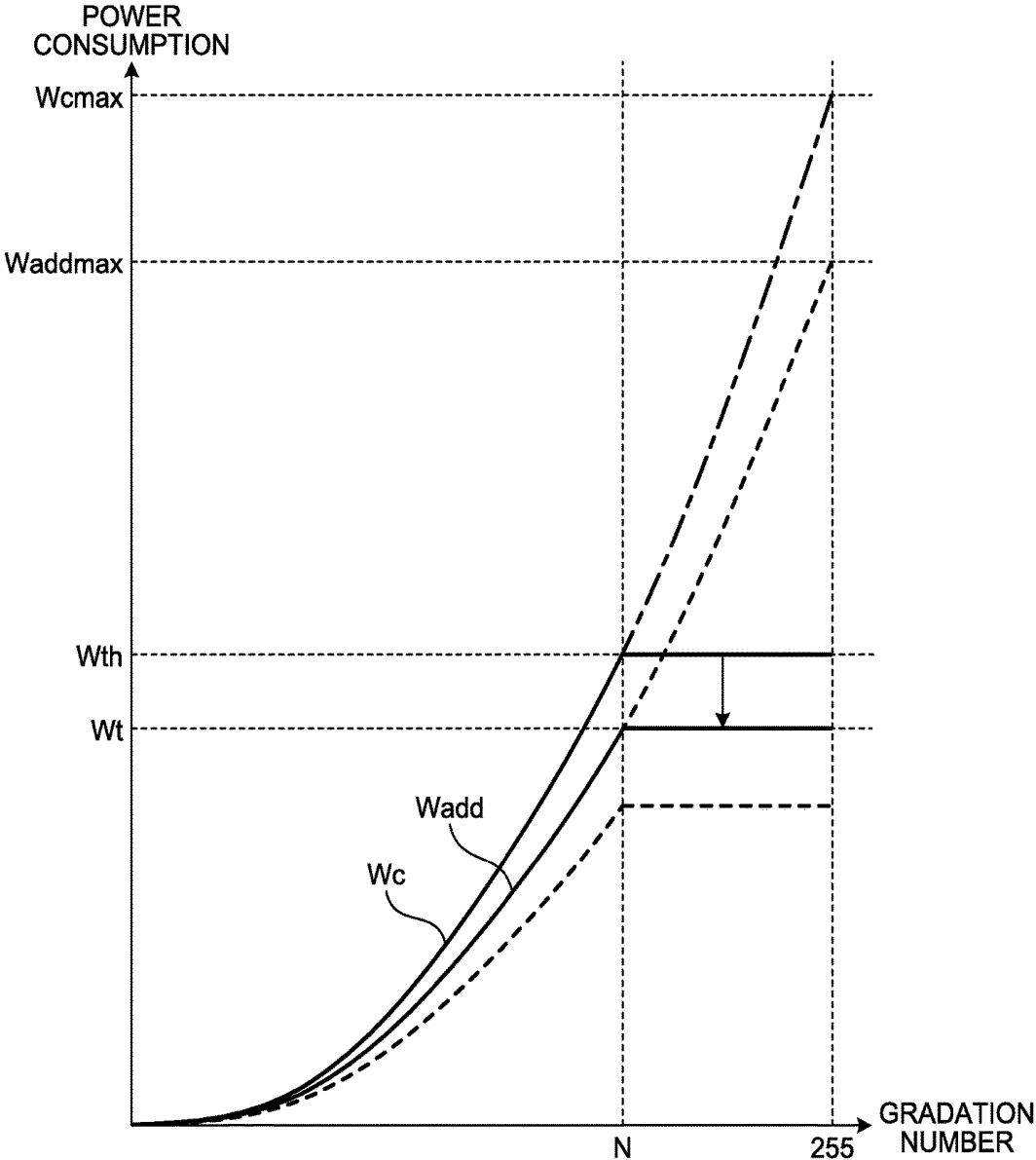


FIG.9

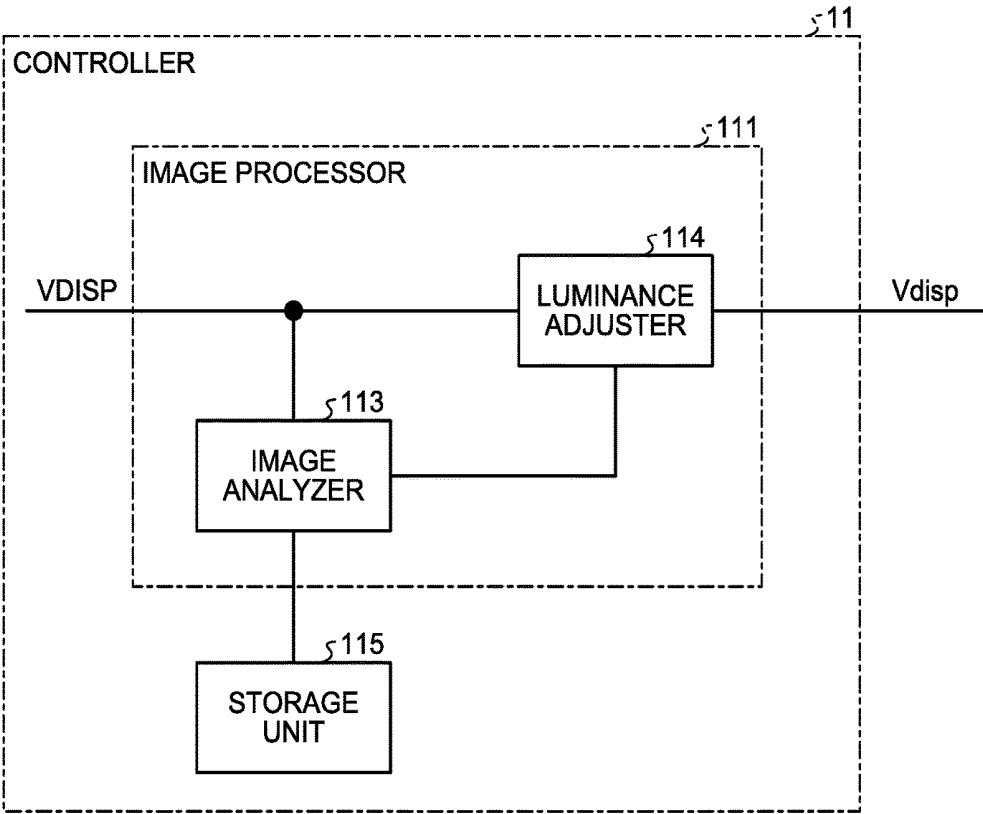


FIG.10

§D1

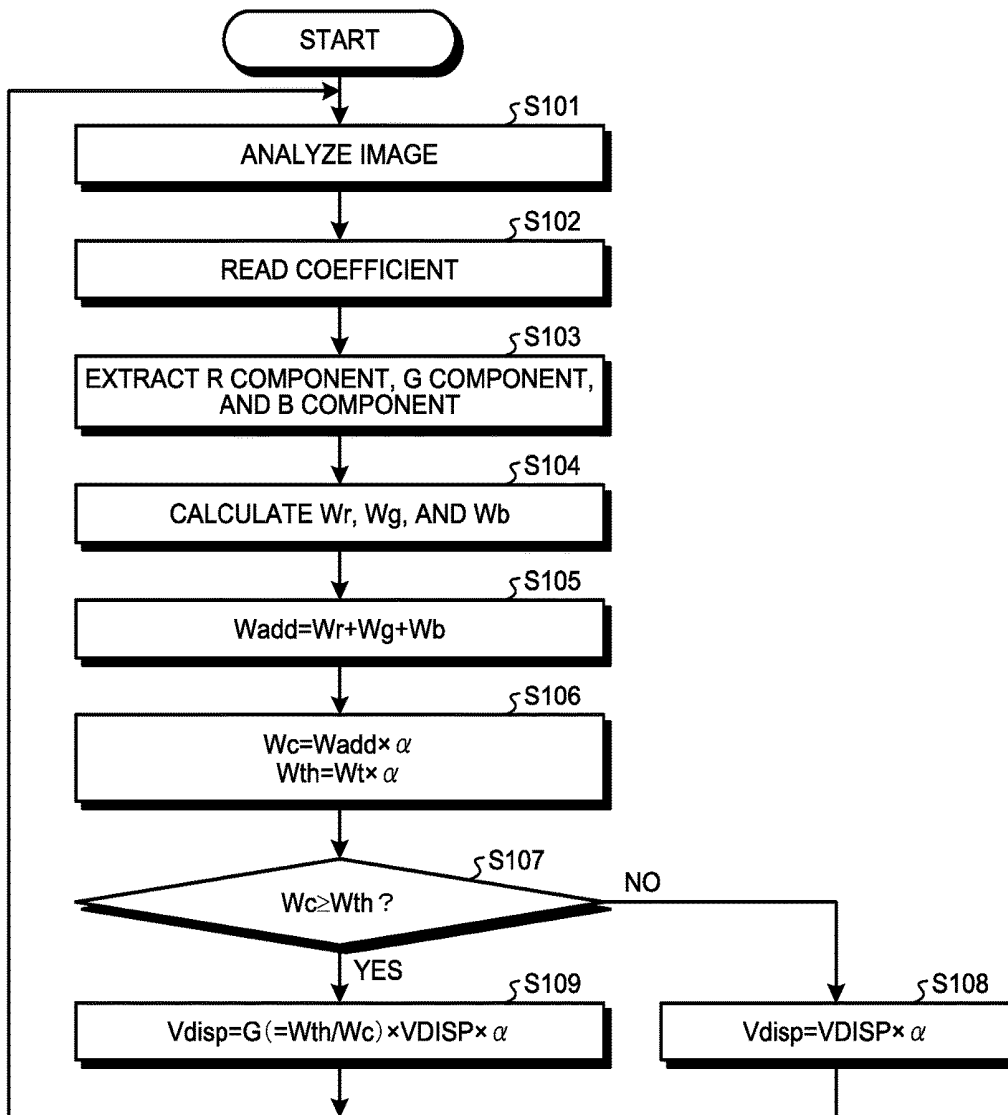
VIDEO SIGNAL	COEFFICIENT
SINGLE-COLOR RASTER (R)	$\alpha 1 (=1)$
SINGLE-COLOR RASTER (G)	$\alpha 1 (=1)$
SINGLE-COLOR RASTER (B)	$\alpha 1 (=1)$
COMPLEMENTARY COLOR RASTER (Y)	$\alpha 2$
COMPLEMENTARY COLOR RASTER (M)	$\alpha 2$
COMPLEMENTARY COLOR RASTER (C)	$\alpha 2$
WHITE RASTER (W)	$\alpha 3$
NATURAL IMAGE (PATTERN 1)	$\alpha 4-1$
NATURAL IMAGE (PATTERN 2)	$\alpha 4-2$
NATURAL IMAGE (PATTERN 3)	$\alpha 4-3$
:	:
NATURAL IMAGE (PATTERN p)	$\alpha 4-p$

FIG.11

§D2

VIDEO SIGNAL	MAXIMUM POWER VALUE
SINGLE-COLOR RASTER (R)	W_{rmax}
SINGLE-COLOR RASTER (G)	W_{gmax}
SINGLE-COLOR RASTER (B)	W_{bmax}

FIG.12



DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims priority from Japanese Application No. 2017-171879, filed on Sep. 7, 2017, the contents of which are incorporated by reference herein in its entirety.

BACKGROUND

1. Technical Field

[0002] The present disclosure relates to a display device.

2. Description of the Related Art

[0003] Recent years have seen a growing demand for display devices each using a liquid crystal display panel or an organic electroluminescent display (OLED) panel that uses organic electroluminescence. For electronic apparatuses typified by portable information apparatuses, a need for technology to reduce power consumption is increasing. For example, since an electronic apparatus having a display device consumes large power for driving the display device, the power consumption required for driving the display device is desired to be reduced.

[0004] Organic electroluminescent (EL) elements constituting pixels of the OLED are self-luminous elements, and do not need an illuminating member, such as a backlight. Therefore, the power consumption can be reduced.

SUMMARY

[0005] A display device according to one aspect includes an electroluminescent (EL) panel comprising a plurality of first light-emitting elements configured to emit a first color, a plurality of second light-emitting elements configured to emit a second color, and a plurality of third light-emitting elements configured to emit a third color, an image analyzer configured to obtain, in displaying of a received video signal, a first power serving as a total value of a power required for displaying the first color, a power required for displaying the second color, and a power required for displaying the third color, and configured to calculate a second power by multiplying the first power by a predetermined coefficient according to the video signal, and calculate a threshold power by multiplying, by the coefficient, a maximum allowable power that is allowed when the EL panel performs image display, and a luminance adjuster configured to multiply the video signal by a ratio between the threshold power and the second power when the second power is equal to or greater than the threshold power.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a block diagram illustrating a configuration example of a display device according to an embodiment of the present disclosure;

[0007] FIG. 2 is a diagram illustrating an exemplary configuration of elements including an equivalent circuit of a pixel of an organic electroluminescent (EL) panel for the display device according to the embodiment;

[0008] FIG. 3 is a timing diagram for control signals in the display device according to the embodiment;

[0009] FIG. 4 is a diagram illustrating an equivalent circuit of each pixel of the organic EL panel;

[0010] FIG. 5 is a diagram illustrating an equivalent circuit in a case where two sub-pixels in the equivalent circuit illustrated in FIG. 4 are simultaneously supplied with video signals having the same gradation as that of FIG. 4;

[0011] FIG. 6 is a diagram illustrating an equivalent circuit in a case where one sub-pixel in the equivalent circuit illustrated in FIG. 4 is supplied with a video signal having the same gradation as that of FIG. 4;

[0012] FIG. 7 is a diagram illustrating relations between a display gradation and power consumption during white raster display;

[0013] FIG. 8 is a diagram illustrating an exemplary result of luminance adjustment in the case of the white raster display in the display device according to the embodiment;

[0014] FIG. 9 is a diagram illustrating an exemplary circuit block configuration for performing the luminance adjustment according to the embodiment;

[0015] FIG. 10 is a diagram illustrating an example of coefficient information including coefficients for respective patterns of the video signal;

[0016] FIG. 11 is a diagram illustrating an example of maximum power value information including maximum power values for respective colors each required for displaying a single-color raster at the maximum gradation level; and

[0017] FIG. 12 is a flowchart illustrating an exemplary luminance adjustment procedure according to the embodiment.

DETAILED DESCRIPTION

[0018] The following describes an embodiment of the present disclosure with reference to the drawings. The disclosure is merely an example, and the present disclosure naturally encompasses appropriate modifications easily conceivable by those skilled in the art while maintaining the gist of the disclosure. To further clarify the description, widths, thicknesses, shapes, and the like of various parts are schematically illustrated in the drawings as compared with actual aspects thereof, in some cases. However, they are merely examples, and interpretation of the present disclosure is not limited thereto. The same element as that illustrated in a drawing that has already been discussed is denoted by the same reference numeral throughout the description and the drawings, and detailed description thereof will not be repeated in some cases where appropriate. The power consumption, however, increases with increase in luminance of a display screen. Hence, for example, a function is provided in which a threshold is set for the total power consumption of all lines constituting one frame, and the luminance is automatically adjusted when the total power consumption is equal to or higher than the threshold (such as Japanese Patent Application Laid-open Publication No. 2016-033607 A). In the above-described technology, the luminance cannot be appropriately adjusted depending on the video signal, and power may exceed a maximum allowable power that is allowed when the display device displays an image. It is an object of the present disclosure to provide a display device capable of appropriately adjusting the luminance regardless of the video signal.

[0019] FIG. 1 is a block diagram illustrating a configuration example of a display device according to the embodiment. As illustrated in FIG. 1, a display device 1 according

to the embodiment includes a controller **11** and an organic electroluminescent (EL) panel **10**. Pixels Pix having thin-film transistors (TFTs) and organic electroluminescent (EL) elements are arranged in a matrix in a display region **20** of the organic EL panel **10**. Other electroluminescent (EL) elements, such as μ (micro) LED and so on, can be applied in replace of organic electroluminescent (EL) elements. In the display region **20**, a row denotes an array in the horizontal direction, and a column denotes an array in the vertical direction. FIG. 1 illustrates an example in which m (where m is a natural number) pixels Pix are arranged in the row direction, and n (where n is a natural number) pixels Pix are arranged in the column direction.

[0020] In the present embodiment, each of the pixels Pix includes three sub-pixels Rpix, Gpix, and Bpix. The three sub-pixels Rpix, Gpix, and Bpix included in the pixel Pix have luminescent colors of, for example, red (R), green (G), and blue (B), respectively, and serve as the pixel Pix as one-unit pixel constituted by three sub-pixels. Light-emitting elements (organic EL elements) constitute the sub-pixels Rpix, Gpix, and Bpix. In the present embodiment, the light-emitting elements are organic light-emitting diodes. The organic EL panel **10** uses a video signal driver **100** and a scan signal driver **200** to generate signals for controlling light emission of the light-emitting elements, and thus displays an image.

[0021] The controller **11** controls the video signal driver **100** and the scan signal driver **200** based on a video signal supplied from, for example, an external host integrated circuit (IC) (not illustrated). The controller **11** is included in, for example, an integrated circuit (IC), and supplies control signals to the video signal driver **100** and the scan signal driver **200** to control them so as to operate in synchronization with each other.

[0022] The controller **11** includes a clock generator (not illustrated) for generating a reference clock. The controller **11** is configured to generate the control signals to be supplied to the video signal driver **100** and the scan signal driver **200** based on the reference clock generated by the clock generator.

[0023] The video signal driver **100** is an IC that generates video voltages to be applied to each of the pixels Pix. The scan signal driver **200** is an IC that generates gate voltages to be applied to the thin-film transistor (TFT) elements. The TFT elements are included in each of the pixels Pix for selecting pixels to be applied with the video voltages. The video signal driver **100** and the scan signal driver **200** are illustrated in FIG. 1 as components different from each other, but may be incorporated in one IC, or may be constituted by a circuit directly provided on a substrate.

[0024] The video signal driver **100** is coupled to video signal lines **110**, **120**, and **130** traversing in the column direction in the display region **20**. The video signal lines **110** are common to corresponding ones of the sub-pixels Rpix arranged in the column direction. The video signal lines **120** are common to corresponding ones of the sub-pixels Gpix arranged in the column direction. The video signal lines **130** are common to corresponding ones of the sub-pixels Bpix arranged in the column direction. The video signal lines **110**, **120**, and **130** are coupled to pixel switches included in the sub-pixels Rpix, Gpix, and Bpix, respectively. An equivalent circuit of the pixel Pix including the pixel switches will be described in detail with reference to the diagrams below.

[0025] The scan signal driver **200** is coupled to scan signal lines **210**, light emission control lines **220**, and power supply lines **230** traversing in the row direction in the display region **20**. Each of the scan signal lines **210**, each of the light emission control lines **220**, and each of the power supply lines **230** are common to corresponding ones of the pixels Pix arranged in the row direction.

[0026] The organic EL panel **10** includes high-potential supply lines **310** (first reference voltage) and low-potential supply lines **320** (second reference voltage). The potential of the high-potential supply lines **310** is denoted as a high-potential voltage V_{dd}. The potential of the low-potential supply lines **320** is denoted as a low-potential voltage V_{ss}. The high-potential supply lines **310** and the low-potential supply lines **320** are common to all the pixels Pix constituting the display region **20** or some of the pixels Pix. The high-potential supply lines **310** and the low-potential supply lines **320** give potential differences for causing the light-emitting elements in the sub-pixels Rpix, Gpix, and Bpix of the respective pixels Pix to emit light.

[0027] FIG. 2 is a diagram illustrating an exemplary configuration of elements including the equivalent circuit of a pixel of the organic EL panel for the display device according to the embodiment. FIG. 2 illustrates the exemplary configuration of one of the pixels Pix constituting the display region **20**.

[0028] As described above, in the present embodiment, the pixel Pix includes the three sub-pixels Rpix, Gpix, and Bpix. The three sub-pixels Rpix, Gpix, and Bpix correspond to the luminescent colors of, for example, red (R), green (G), and blue (B). The three sub-pixels Rpix, Gpix, and Bpix share a light emission control switch **31**.

[0029] The controller **11** includes an image processor **111** and a timing controller **112**.

[0030] The image processor **111** applies various types of image processing to a video signal V_{disp}. The image processing applied by the image processor **111** includes, for example, gamma conversion or the like. In the present embodiment, the image processing includes at least luminance adjustment processing of the video signal V_{disp}. The luminance adjustment processing according to the present embodiment will be described later. The present disclosure is not limited by image processing other than the luminance adjustment processing applied by the image processor **111**.

[0031] The timing controller **112** generates the control signals including a first timing pulse LP1, a second timing pulse LP2, a third timing pulse LP3, an initialization voltage output timing control signal xasw1, a video voltage output timing control signal xasw2, a light emission control signal BG, and a reset control signal RG based on the video signal V_{disp}.

[0032] The video signal driver **100** generates video voltages V_{sigR}, V_{sigG}, and V_{sigB} based on the video signal V_{disp} received from the controller **11**.

[0033] The video signal driver **100** includes initialization signal control switches **101**, **103**, and **105** and video voltage control switches **102**, **104**, and **106**.

[0034] The initialization signal control switch **101** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **110**, and is supplied, at the other thereof (second terminal), with an initialization voltage V_{ini}. The gate (third terminal) of the initialization signal control switch **101** receives the initialization voltage output timing control signal xasw1.

[0035] The initialization signal control switch **103** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **120**, and is supplied, at the other thereof (second terminal), with the initialization voltage V_{ini} . The gate (third terminal) of the initialization signal control switch **103** receives the initialization voltage output timing control signal $xasw1$. The initialization signal control switch **105** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **130**, and is supplied, at the other thereof (second terminal), with the initialization voltage V_{ini} . The gate (third terminal) of the initialization signal control switch **105** receives the initialization voltage output timing control signal $xasw1$.

[0036] In the present embodiment, each of the initialization signal control switches **101**, **103**, and **105** is, for example, a transistor. When the initialization voltage output timing control signal $xasw1$ is applied to the gates of the initialization signal control switches **101**, **103**, and **105**, the initialization signal control switches **101**, **103**, and **105** are brought into the conductive state, and the initialization voltage V_{ini} is applied to the video signal lines **110**, **120**, and **130**.

[0037] The video voltage control switch **102** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **110**, and is supplied, at the other thereof (second terminal), with the video voltage V_{sigR} . The gate (third terminal) of the video voltage control switch **102** receives the video voltage output timing control signal $xasw2$.

[0038] The video voltage control switch **104** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **120**, and is supplied, at the other thereof (second terminal), with the video voltage V_{sigG} . The gate (third terminal) of the video voltage control switch **104** receives the video voltage output timing control signal $xasw2$.

[0039] The video voltage control switch **106** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **130**, and is supplied, at the other thereof (second terminal), with the video voltage V_{sigB} . The gate (third terminal) of the video voltage control switch **106** receives the video voltage output timing control signal $xasw2$.

[0040] In the present embodiment, each of the video voltage control switches **102**, **104**, and **106** is, for example, a transistor. When the video voltage output timing control signal $xasw2$ is applied to the gate of the video voltage control switch **102**, the video voltage control switch **102** is brought into the conductive state, and the video voltage V_{sigR} is applied to the video signal line **110**. When the video voltage output timing control signal $xasw2$ is applied to the gate of the video voltage control switch **104**, the video voltage control switch **104** is brought into the conductive state, and the video voltage V_{sigG} is applied to the video signal line **120**. When the video voltage output timing control signal $xasw2$ is applied to the gate of the video voltage control switch **106**, the video voltage control switch **106** is brought into the conductive state, and the video voltage V_{sigB} is applied to the video signal line **130**. In the present embodiment, the video voltages V_{sigR} , V_{sigG} , and V_{sigB} are gradation signals corresponding to the video signal V_{disp} .

[0041] The scan signal driver **200** includes a reset control switch **235**.

[0042] The reset control switch **235** is coupled, at one of the source and the drain (first terminal) thereof, to the power supply line **230**, and is supplied, at the other thereof (second terminal), with a reset voltage V_{rst} . The gate (third terminal) of the reset control switch **235** receives the reset control signal RG . In the present embodiment, the reset control switch **235** is, for example, a transistor. When the reset control signal RG is applied to the gate of the reset control switch **235**, the reset control switch **235** is brought into the conductive state, and the reset voltage V_{rst} is applied to the power supply line **230**.

[0043] The pixel **Pix** includes the sub-pixels R_{pix} , G_{pix} , and B_{pix} and the light emission control switch **31**.

[0044] The light emission control switch **31** is coupled, at one of the source and the drain (first terminal) thereof, to corresponding one of the high-potential supply lines **310**. The gate (third terminal) of the light emission control switch **31** is coupled to the light emission control line **220**. In the present embodiment, the light emission control switch **31** is, for example, a TFT element.

[0045] The sub-pixel R_{pix} includes a pixel switch **331**, a drive transistor **341**, an organic light-emitting diode **371**, a storage capacitor **351**, and an additional capacitor **361**.

[0046] The pixel switch **331** is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line **110**. The gate (third terminal) of the pixel switch **331** is coupled to the scan signal line **210**. In the present embodiment, the pixel switch **331** is, for example, a TFT element.

[0047] The drive transistor **341** is coupled, at one of the source and the drain (first terminal) thereof, to the anode of the organic light-emitting diode **371**, and is coupled, at the other thereof (second terminal), to the power supply line **230** and the other of the source and the drain (second terminal) of the light emission control switch **31**. The gate (third terminal) of the drive transistor **341** is coupled to the other of the source and the drain (second terminal) of the pixel switch **331**. In the present embodiment, the drive transistor **341** is, for example, an n-channel transistor. However, a p-channel transistor can be used according to circuit configuration.

[0048] In the present embodiment, the storage capacitor **351** is coupled between the source and the gate (third terminal) of the drive transistor **341**. In the present embodiment, the additional capacitor **361** is coupled between the source of the drive transistor **341** and corresponding one of the low-potential supply lines **320**, corresponding one of the high-potential supply lines **310**, or a predetermined reference voltage. In the present embodiment, the additional capacitor **361** may be provided between the source of the drive transistor **341** and the low-potential supply line **320**, and between the source (first terminal) of the drive transistor **341** and the high-potential supply line **310**. However, one terminal of the additional capacitor **361** can be coupled to the drain of the driver transistor **341** instead of the source, according to circuit configuration.

[0049] When a scan voltage SG is applied from the scan signal driver **200** to the scan signal line **210**, the pixel switch **331** is brought into the conductive state. In the case where the pixel switch **331** is in the conductive state, when the video voltage V_{sigR} is applied from the video signal driver **100** to the video signal line **110**, the video voltage V_{sigR} is applied to the gate (third terminal) of the drive transistor **341**.

[0050] The drive transistor 341 controls the current value supplied to the organic light-emitting diode 371 according to the voltage between the gate and the source of the drive transistor 341.

[0051] When the voltage is applied to the gate (third terminal) of the drive transistor 341, an electric charge is stored in the storage capacitor 351. After the electric charge for delivering a predetermined current to the drive transistor 341 is stored in the storage capacitor 351, the pixel switch 331 is brought into the non-conductive state to maintain the voltage between the gate and the source of the drive transistor 341. A current corresponding to the voltage between the gate and the source of the drive transistor 341 flows therein. The current between the drain and the source of the drive transistor 341 flows in the organic light-emitting diode 371, and the organic light-emitting diode 371 emits light at luminance corresponding to the current value.

[0052] The additional capacitor 361 coupled to the source of the drive transistor 341 has a role of setting the voltage between the gate (third terminal) and the source of the drive transistor 341 according to the voltage level of the video voltage VsigR through capacitance division with the storage capacitor 351. Specifically, the capacitance of the additional capacitor 361 is often set to be larger than the capacitance of the storage capacitor 351 to increase the setting range of the voltage between the gate (third terminal) and the source (first terminal) of the drive transistor 341.

[0053] The cathode of the organic light-emitting diode 371 is coupled to the low-potential supply line 320. In the case where the drive transistor 341 is in the conductive state, after the light emission control switch 31 is brought into the conductive state, a current corresponding to the voltage between the gate and the source of the drive transistor 341 flows in the organic light-emitting diode 371, and the organic light-emitting diode 371 emits light.

[0054] The sub-pixel Gpix includes a pixel switch 332, a drive transistor 342, an organic light-emitting diode 372, a storage capacitor 352, and an additional capacitor 362.

[0055] The pixel switch 332 is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line 120. The gate (third terminal) of the pixel switch 332 is coupled to the scan signal line 210. In the present embodiment, the pixel switch 332 is, for example, a TFT element.

[0056] The drive transistor 342 is coupled, at one of the source and the drain (first terminal) thereof, to the anode of the organic light-emitting diode 372, and is coupled, at the other thereof (second terminal), to the power supply line 230 and the other of the source and the drain (second terminal) of the light emission control switch 31. The gate (third terminal) of the drive transistor 342 is coupled to the other of the source and the drain (second terminal) of the pixel switch 332. In the present embodiment, the drive transistor 342 is, for example, an n-channel transistor. However a p-channel transistor can be used according to circuit configuration.

[0057] In the present embodiment, the storage capacitor 352 is coupled between the source and the gate (third terminal) of the drive transistor 342. In the present embodiment, an additional capacitor 362 is coupled between the source and the low-potential supply line 320, the high-potential supply line 310, or the predetermined reference voltage. In the present embodiment, the additional capacitor 362 may be provided between the source of the drive

transistor 342 and the low-potential supply line 320, and between the source of the drive transistor 342 and the high-potential supply line 310. However, one terminal of the additional capacitor 362 can be coupled to the drain of the driver transistor 342 instead of the source, according to circuit configuration.

[0058] When the scan voltage SG is applied from the scan signal driver 200 to the scan signal line 210, the pixel switch 332 is brought into the conductive state. In the case where the pixel switch 332 is in the conductive state, when the video voltage VsigG is applied from the video signal driver 100 to the video signal line 120, the video voltage VsigG is applied to the gate (third terminal) of the drive transistor 342.

[0059] The drive transistor 342 controls the current value supplied to the organic light-emitting diode 372 according to the voltage between the gate and the source of the drive transistor 342. When the voltage is applied to the gate (third terminal) of the drive transistor 342, an electric charge is stored in the storage capacitor 352. After the electric charge for delivering a predetermined current to the drive transistor 342 is stored in the storage capacitor 352, the pixel switch 332 is brought into a non-conduction state to maintain the voltage between the gate and the source of the drive transistor 342. A current corresponding to the voltage between the gate and the source of the drive transistor 342 flows therein. The current between the drain and the source of the drive transistor 342 flows in the organic light-emitting diode 372, and the organic light-emitting diode 372 emits light at luminance corresponding to the current value.

[0060] In the present embodiment, the additional capacitor 362 coupled to the source of the drive transistor 342 has a role of setting the voltage between the gate (third terminal) and the source of the drive transistor 342 according to the voltage level of the video voltage VsigG through capacitance division with the storage capacitor 352. However, one terminal of the additional capacitor 361 can be coupled to the drain of the driver transistor 341 instead of the source, according to circuit configuration. Specifically, the capacitance of the additional capacitor 362 is often set to be larger than the capacitance of the storage capacitor 352 to increase the setting range of the voltage between the gate (third terminal) and the source of the drive transistor 342.

[0061] The cathode of the organic light-emitting diode 372 is coupled to the low-potential supply line 320. In the case where the drive transistor 342 is in the conductive state, after the light emission control switch 31 is brought into the conductive state, a current corresponding to the voltage between the gate and the source of the drive transistor 342 flows in the organic light-emitting diode 372, and the organic light-emitting diode 372 emits light.

[0062] The sub-pixel Bpix includes a pixel switch 333, a drive transistor 343, an organic light-emitting diode 373, a storage capacitor 353, and the additional capacitor 363.

[0063] The pixel switch 333 is coupled, at one of the source and the drain (first terminal) thereof, to the video signal line 130. The gate (third terminal) of the pixel switch 333 is coupled to the scan signal line 210. In the present embodiment, the pixel switch 333 is, for example, a TFT element.

[0064] The drive transistor 343 is coupled, at one of the source and the drain (first terminal) thereof, to the anode of the organic light-emitting diode 373, and is coupled, at the other thereof (second terminal), to the power supply line 230

and the other of the source and the drain (second terminal) of the light emission control switch 31. The gate (third terminal) of the drive transistor 343 is coupled to the other of the source and the drain (second terminal) of the pixel switch 333. In the present embodiment, the drive transistor 343 is, for example, an n-channel transistor. However, a p-channel transistor can be used according to circuit configuration.

[0065] In the present embodiment, the storage capacitor 353 is coupled between the source and the gate (third terminal) of the drive transistor 343. In the present embodiment, the additional capacitor 363 is coupled between the source of the drive transistor 343 and the low-potential supply line 320, the high-potential supply line 310, or the predetermined reference voltage. In the present embodiment, the additional capacitor 363 may be provided both between the source of the drive transistor 343 and the low-potential supply line 320, and between one of the source and the drain (first terminal) of the drive transistor 343 and the high-potential supply line 310. However, one terminal of the additional capacitor 363 can be coupled to the drain of the driver transistor 343 instead of the source, according to circuit configuration.

[0066] When the scan voltage SG is applied from the scan signal driver 200 to the scan signal line 210, the pixel switch 333 is brought into the conductive state. In the case where the pixel switch 333 is in the conductive state, when the video voltage VsigB is applied from the video signal driver 100 to the video signal line 130, the video voltage VsigB is applied to the gate (third terminal) of the drive transistor 343.

[0067] The drive transistor 343 controls the current value supplied to the organic light-emitting diode 373 according to the voltage between the gate and the source of the drive transistor 343. When the voltage is applied to the gate (third terminal) of the drive transistor 343, an electric charge is stored in the storage capacitor 353. After the electric charge for delivering a predetermined current to the drive transistor 343 is stored in the storage capacitor 353, the pixel switch 333 is brought into a non-conduction state to maintain the voltage between the gate and the source of the drive transistor 343. A current corresponding to the voltage between the gate and the source of the drive transistor 343 flows therein. The current between the drain and the source of the drive transistor 343 flows in the organic light-emitting diode 373, and the organic light-emitting diode 373 emits light at luminance corresponding to the current value.

[0068] The additional capacitor 363 coupled to the source of the drive transistor 343 has a role of setting the voltage between the gate (third terminal) and the source of the drive transistor 343 according to the voltage level of the video voltage VsigB through capacitance division with the storage capacitor 353. Specifically, the capacitance of the additional capacitor 363 is often set to be larger than the capacitance of the storage capacitor 353 to increase the setting range of the voltage between the gate (third terminal) and the source of the drive transistor 343.

[0069] The cathode of the organic light-emitting diode 373 is coupled to the low-potential supply line 320. In the case where the drive transistor 343 is in the conductive state, after the light emission control switch 31 is brought into the conductive state, a current corresponding to the voltage between the gate and the source of the drive transistor 343

flows in the organic light-emitting diode 373, and the organic light-emitting diode 373 emits light.

[0070] The light emission control switch 31 controls electrical couplings between the others of the sources and the drains (second terminals) of the drive transistors 341, 342, and 343 and the high-potential supply line 310. In the present embodiment, the light emission control switch 31 is, for example, an n-channel transistor. A p-channel transistor can be used as the light emission control switch instead of n-channel transistor. The gate (third terminal) of the light emission control switch 31 is coupled to the light emission control line 220. When the light emission control signal BG is applied from the scan signal driver 200 to the light emission control line 220, the light emission control switch 31 is brought into the conductive state.

[0071] When the light emission control switch 31 is in the non-conductive state and the reset control switch 235 is in the conductive state, the others of the sources and the drains (second terminals) of the drive transistors 341, 342, and 343 are coupled to the power supply line 230. The reset voltage Vrst is set to a voltage at which no current flows in the organic light-emitting diodes 371, 372, and 373 during a reset condition, and may be set to, for example, the potential of the low-potential supply line 320.

[0072] The equivalent circuit diagram illustrated in FIG. 2 is merely an example. A different circuit may be employed. For example, the light emission control switch 31 may be provided in each of the three sub-pixels Rpix, Gpix, and Bpix.

[0073] Regarding the initialization signal control switches 101, 103, and 105, the video voltage control switches 102, 104, and 106, the reset control switch 235, the pixel switches 331, 332, and 333, the drive transistors 341, 342, and 343, and the light emission control switch 31 described above, which of the source and the drain serves as the first terminal or the second terminal is appropriately selected according to the circuit configurations of the video signal driver 100, the scan signal driver 200, and the sub-pixels Rpix, Gpix, and Bpix.

[0074] The following describes a detailed operation of the display device 1 according to the present embodiment. FIG. 3 is a timing diagram for the control signals in the display device according to the embodiment.

[0075] In the timing diagram illustrated in FIG. 3, the horizontal axis represents time. (a) of FIG. 3 illustrates the initialization voltage Vini or the video voltages VsigR, VsigG, and VsigB supplied from the video signal driver 100 to the first video signal line 110. In the example illustrated in (a) of FIG. 3, the vertical axis represents the level of the initialization voltage Vini or the video voltages VsigR, VsigG, and VsigB. FIG. 3 illustrates the timing diagram in the case where the transistors 101, 102, 103, 104, 105, 106, 235, 31, 331, 341, 332, 342, 333, and 343 are n-channel transistors.

[0076] (b) of FIG. 3 illustrates the initialization voltage output timing control signal xasw1 supplied from the controller 11 to the video signal driver 100. (c) of FIG. 3 illustrates the video voltage output timing control signal xasw2 supplied from the controller 11 to the video signal driver 100. (d) of FIG. 3 illustrates the light emission control signal BG supplied from the controller 11 to the scan signal driver 200. (e) of FIG. 3 illustrates the reset control signal RG supplied from the controller 11 to the scan signal driver 200. (f) of FIG. 3 illustrates the scan voltage SG supplied

from the scan signal driver 200 to the scan signal line 210. In the examples illustrated in (b), (c), (d), (e), and (f) of FIG. 3, the vertical axis represents a logic level “L” or “H” of each of the signals.

[0077] The display operation of the display device 1 according to the present embodiment is performed by raster scanning. In the present embodiment, a plurality of pixel rows constituting the display region 20 of the organic EL panel 10 are sequentially selected from the first row, and the video voltages VsigR, VsigG, and VsigB are written to pixels Pix in the selected row to cause the pixels Pix to emit light, and this operation is repeated for each video signal Vdisp of one frame. The write operation in the present embodiment is divided into a reset operation, an offset cancel operation, and a video voltage write operation.

[0078] The display device 1 according to the present embodiment performs the reset operation, the offset cancel operation, and the video voltage write operation during two horizontal periods (2H) for each pixel row. In the example illustrated in FIG. 3, one horizontal period (1H) is divided into a first period and a second period. For each pixel row, the reset operation is performed during the first period of earlier one horizontal period (1H) (hereinafter, also called the first horizontal period). Subsequently, the offset cancel operation is performed during the first period of later one horizontal period (1H) (hereinafter, also called the second horizontal period), and the video voltage write operation is performed during the subsequent second period of the second horizontal period.

[0079] In the example illustrated in FIG. 3, a period from time t11 to time t17 serves as the first horizontal period, a period from time t11 to time t16 as the first period in the first horizontal period, a period from time t16 to time t17 as the second period in the first horizontal period, a period from time t17 to time t22 as the first period in the second horizontal period, and a period from time t22 to time t27 as the second period in the second horizontal period.

[0080] The reset operation will first be described.

[0081] The light emission control signal BG is controlled to change from “H” to “L” at time t11 of the first horizontal period, and the logic level of the reset control signal RG is controlled to change from “L” to “H” at the subsequent time t12. Then, the reset control switch 235 is brought into the conductive state, and the reset voltage Vrst is supplied to the power supply line 230, and applied to the others of the sources and the drains (second terminals) of the drive transistors 341, 342, and 343. At this time, the logic level of the initialization voltage output timing control signal xasw1 is controlled to change from “L” to “H” in synchronization with the reset control signal RG. Then, the initialization signal control switches 101, 103, and 105 are brought into the conductive state, and the video signal driver 100 starts loading data of the initialization voltage Vini to supply the initialization voltage Vini to the video signal lines 110, 120, and 130.

[0082] At the subsequent time t13, the logic level of the scan voltage SG is controlled to change from “L” to “H”. Then, the pixel switches 331, 332, and 333 are brought into the conductive state, and the initialization voltage Vini is applied to the gates (third terminals) of the drive transistors 341, 342, and 343 through the pixel switches 331, 332, and 333.

[0083] As a result, the potentials of the gates (third terminals) of the drive transistors 341, 342, and 343 are

initialized to a potential corresponding to the initialization voltage Vini. The drive transistors 341, 342, and 343 are brought into the conductive state. Consequently, the potentials of the sources of the drive transistors 341, 342, and 343 are reset to a potential corresponding to the reset voltage Vrst, and the voltages across terminals of the storage capacitors 351, 352, and 353 are set to a voltage corresponding to (Vini-Vrst). A voltage corresponding to (Vrst-Vss) is applied to the organic light-emitting diodes 371, 372, and 373. The reset voltage Vrst is set such that the voltage applied to the organic light-emitting diodes 371, 372, and 373 is equal to or lower than a light emission threshold voltage (light emission start voltage) of the organic light-emitting diodes 371, 372, and 373. For example, the light emission threshold voltage is a voltage at which a current starts flowing in each of the organic light-emitting diodes 371, 372, and 373, that is, a forward voltage drop.

[0084] Then, the logic level of the scan voltage SG is controlled to change from “H” to “L” at time t14. Then, the pixel switches 331, 332, and 333 are brought into the non-conductive state, and the reset operation ends. At the subsequent time t15, the logic level of the initialization voltage output timing control signal xasw1 is controlled to change from “H” to “L”. Then, the initialization signal control switches 101, 103, and 105 are brought into the non-conductive state, and the video signal driver 100 stops loading the data of the initialization voltage Vini. The period from time t13 to time t14 in the first period of the first horizontal period is hereinafter called a “reset period”.

[0085] The following describes the offset cancel operation.

[0086] The logic level of the reset control signal RG is controlled to change from “H” to “L” at time t17 of the second horizontal period, and the logic level of the light emission control signal BG is controlled to change from “L” to “H” at the subsequent time t18. Then, the light emission control switch 31 is brought into the conductive state, and the high-potential voltage Vdd is supplied to the power supply line 230, and applied to the drains (second terminals) of the drive transistors 341, 342, and 343 in this embodiment. At this time, the logic level of the initialization voltage output timing control signal xasw1 is controlled to change from “L” to “H” in synchronization with the light emission control signal BG. Then, the initialization signal control switches 101, 103, and 105 are brought into the conductive state, and the video signal driver 100 starts loading the data of the initialization voltage Vini to supply the initialization voltage Vini to the video signal lines 110, 120, and 130.

[0087] At the subsequent time t19, the logic level of the scan voltage SG is controlled to change from “L” to “H”. Then, the pixel switches 331, 332, and 333 are brought into the conductive state, and the initialization voltage Vini is applied to the gates (third terminals) of the drive transistors 341, 342, and 343 through the pixel switches 331, 332, and 333.

[0088] As a result, the potentials of the gates (third terminals) of the pixel switches 331, 332, and 333 are fixed to a potential corresponding to the initialization voltage Vini. Since the light emission control switch 31 is in the conductive state, currents flow into the drive transistors 341, 342, and 343 from the high-potential supply line 310, and the potentials of ones of the sources and the drains (first terminals) of the drive transistors 341, 342, and 343 rise from the reset voltage Vrst that has been written in the reset operation.

In this embodiment, the potentials of the sources of the drive transistors **341**, **342**, and **343** reach a potential ($V_{ini}-V_{th}$) that is lower by a threshold voltage V_{th} than the potentials of the gates (third terminals) thereof. Then, the pixel switches **331**, **332**, and **333** are brought into the non-conductive state by controlling the scan voltage SG from “H” to “L”. At this time, the potentials of the sources are fixed to ($V_{ini}-V_{th}$) in this embodiment. The voltages across the terminals of the storage capacitors **351**, **352**, and **353** are set to a voltage corresponding to the threshold voltage V_{th} . Assuming this state as a reference, voltages corresponding to the video voltages V_{sigR} , V_{sigG} , and V_{sigB} are written to the storage capacitors **351**, **352**, and **353** in the video voltage write operation to be described later. This operation cancels the influence of a pixel-to-pixel variation in the threshold voltage V_{th} among the drive transistors **341**, **342**, and **343** on the currents flowing in the organic light-emitting diodes **371**, **372**, and **373** during the light-emitting operations.

[0089] At time t_{20} , the logic level of the scan voltage SG is controlled to change from “H” to “L”. Then, the pixel switches **331**, **332**, and **333** are brought into the non-conductive state, and the offset cancel operation ends. At the subsequent time t_{21} , the logic level of the initialization voltage output timing control signal $xasw1$ is controlled to change from “H” to “L”. Then, the initialization signal control switches **101**, **103**, and **105** are brought into the non-conductive state, and the video signal driver **100** stops loading the data of the initialization voltage V_{ini} . The period from time t_{19} to time t_{20} in the first period of the second horizontal period is hereinafter called an “offset cancel period”. At the subsequent time t_{22} the logic level of the scan voltage SG is controlled to change from “H” to “L” at the timing of t_{22} to shunt the high-potential voltage V_{dd} .

[0090] The following describes the video voltage write operation.

[0091] The logic level of the reset control signal RG is maintained at “L” and the logic level of the light emission control signal BG is maintained at “L” during a video voltage write period.

[0092] At time t_{23} of the second horizontal period, the logic level of the video voltage output timing control signal $xasw2$ is controlled to change from “L” to “H”. Then, the video voltage control switches **102**, **104**, and **106** are brought into the conductive state to supply the video voltage V_{sigR} to the video signal line **110**, the video voltage V_{sigG} to the video signal line **120**, and the video voltage V_{sigB} to the video signal line **130**. At the subsequent time t_{24} , the logic level of the scan voltage SG is controlled to change from “L” to “H”. Then, the pixel switches **331**, **332**, and **333** are brought into the conductive state. This operation raises the potential of the gate (third terminal) of the drive transistor **341** from the potential corresponding to the initialization voltage V_{ini} to a potential corresponding to the video voltage V_{sigR} , the potential of the gate (third terminal) of the drive transistor **342** from the potential corresponding to the initialization voltage V_{ini} to a potential corresponding to the video voltage V_{sigG} , and the potential of the gate (third terminal) of the drive transistor **343** from the potential corresponding to the initialization voltage V_{ini} to a potential corresponding to the video voltage V_{sigB} .

[0093] At time t_{25} , the logic level of the scan voltage SG is controlled to change from “H” to “L”. Then, the pixel switches **331**, **332**, and **333** are brought into the non-

conductive state, and the video voltage write operation in the second period of the second horizontal period ends. At the subsequent time t_{26} , the logic level of the video voltage output timing control signal $xasw2$ is controlled to change from “H” to “L”. Then, the video signal driver **100** stops loading the data of the video voltages V_{sigR} , V_{sigG} , and V_{sigB} . The period from time t_{24} to time t_{25} in the second period of the second horizontal period is hereinafter called a “video voltage write period”. During the video voltage write period, the write operation is performed by writing the video voltage V_{sigR} to the sub-pixel R_{pix} , the video voltage V_{sigG} to the sub-pixel G_{pix} , and the video voltage V_{sigB} to the sub-pixel B_{pix} .

[0094] After the video voltage write period described above, the logic level of the light emission control signal BG is controlled to change from “L” to “H” after the time t_{26} . And the organic light-emitting diodes **371**, **372**, and **373** perform the light-emitting operations.

[0095] The display device **1** according to the present embodiment performs the display operation of the video signal V_{disp} for one frame by performing the reset operation, the offset cancel operation, and the video voltage write operation described above by sequentially shifting these operations by one horizontal period (1H) for each pixel row.

[0096] The following describes the luminance adjustment function in the organic EL panel **10** using the organic electroluminescent (EL) elements as the light-emitting elements.

[0097] In the organic EL panel **10** using the organic electroluminescent (EL) elements as the light-emitting elements, the power consumption increases with increase in luminance of the image displayed in the display region **20**. In particular, in some cases of performing white raster display in which the sub-pixels R_{pix} , G_{pix} , and B_{pix} of all the pixels are lit up, complementary color raster display of yellow (Y) in which the sub-pixels R_{pix} and G_{pix} of all the pixels are lit up, the complementary color raster display of magenta (M) in which the sub-pixels R_{pix} and B_{pix} of all the pixels are lit up, or the complementary color raster display of cyan (C) in which the sub-pixels G_{pix} and B_{pix} of all the pixels are lit up, power may exceed a maximum allowable power that is allowed when the organic EL panel **10** performs the image display. Hence, in the present embodiment, to satisfy the maximum allowable power of the organic EL panel **10**, the luminance adjustment function in accordance with the video signal is provided.

[0098] FIG. **4** is a diagram illustrating an equivalent circuit of each pixel of the organic EL panel. In the example illustrated in FIG. **4**, Tr denotes each of the drive transistors of the sub-pixels R_{pix} , G_{pix} , and B_{pix} constituting the pixel; D denotes the organic light-emitting diode; and R denotes a parasitic resistance value of the low-potential supply line **320** coupled to the sub-pixels R_{pix} , G_{pix} , and B_{pix} . FIG. **4** assumes a case where the three sub-pixels R_{pix} , G_{pix} , and B_{pix} are simultaneously supplied with video voltages having the same gradation.

[0099] FIG. **5** is a diagram illustrating an equivalent circuit in a case where two of the sub-pixels in the equivalent circuit illustrated in FIG. **4** are simultaneously supplied with video signals having the same gradation as that of FIG. **4**. FIG. **5** assumes a case where two of the three sub-pixels R_{pix} , G_{pix} , and B_{pix} are simultaneously supplied with video voltages having the same gradation as that of FIG. **4**.

[0100] FIG. 6 is a diagram illustrating an equivalent circuit in a case where one of the sub-pixels in the equivalent circuit illustrated in FIG. 4 is supplied with a video signal having the same gradation as that of FIG. 4. FIG. 6 assumes a case where any one of the three sub-pixels Rpix, Gpix, and Bpix is supplied with a video voltage having the same gradation as that of FIGS. 4 and 5.

[0101] A current value I_1 that flows when the three sub-pixels Rpix, Gpix, and Bpix are simultaneously supplied with the video signals having the same gradation (FIG. 4) is greater than a current value I_3 that flows when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6) ($I_1 > I_3$). Therefore, when the three sub-pixels Rpix, Gpix, and Bpix are simultaneously supplied with the video signals having the same gradation (FIG. 4), the potential on the cathode side of the organic light-emitting diode D is higher than that when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6). As a result, a relation represented by Expression (1) below holds between the current value I_1 that flows when the three sub-pixels Rpix, Gpix, and Bpix are simultaneously supplied with the video signals having the same gradation (FIG. 4) and the total current value $3I_3$ that flows when each of the three sub-pixels Rpix, Gpix, and Bpix is individually supplied with the video signal having the same gradation as that of FIG. 4.

$$I_1 < 3I_3 \quad (1)$$

[0102] When the three sub-pixels Rpix, Gpix, and Bpix are simultaneously supplied with the video signals having the same gradation (FIG. 4), the potential on the cathode side of the organic light-emitting diode D is higher than that when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6). As a result, a relation represented by Expression (2) below holds between a power consumption P_1 obtained when the three sub-pixels Rpix, Gpix, and Bpix are simultaneously supplied with the video signals having the same gradation (FIG. 4) and a total power consumption $3P_3$ obtained when each of the three sub-pixels Rpix, Gpix, and Bpix is individually supplied with the video signal having the same gradation as that of FIG. 4.

$$P_1 < 3P_3 \quad (2)$$

[0103] A current value I_2 that flows when two of the sub-pixels are simultaneously supplied with the video signals having the same gradation as that of FIG. 4 (FIG. 5) is greater than the current value I_3 that flows when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6) ($I_2 > I_3$). Therefore, when two of the sub-pixels are simultaneously supplied with the video signals having the same gradation (FIG. 5), the potential on the cathode side of the organic light-emitting diode D is higher than that when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6). As a result, a relation represented by Expression (3) below holds between the current value I_2 that flows when two of the sub-pixels are simultaneously supplied with the video signals having the same gradation as that of FIG. 4 (FIG. 5) and the total current value $2I_3$ that flows when each of the two of the sub-pixels are individually

supplied with the video signal having the same gradation as that of FIG. 4.

$$I_2 < 2I_3 \quad (3)$$

[0104] When two of the sub-pixels are simultaneously supplied with the video signals having the same gradation as that of FIG. 4 (FIG. 5), the potential on the cathode side of the organic light-emitting diode D is higher than that when one of the sub-pixels is supplied with the video signal having the same gradation as that of FIG. 4 (FIG. 6). As a result, a relation represented by Expression (4) below holds between a power consumption P_2 obtained when two of the sub-pixels are simultaneously supplied with the video signals having the same gradation as that of FIG. 4 (FIG. 5) and the total power consumption $2P_3$ obtained when each of the two of the sub-pixels are individually supplied with the video signal having the same gradation as that of FIG. 4.

$$P_2 < 2P_3 \quad (4)$$

[0105] That is, when a plurality of sub-pixels are simultaneously supplied with video signals, the power consumption is smaller than the total power consumption obtained when each of the sub-pixels is individually supplied with one of the video signals. During the white raster display, a current flows from a plurality of pixels each including the three sub-pixels Rpix, Gpix, and Bpix into the parasitic resistance of the low-potential supply line 320. The following describes a specific example of the luminance adjustment during the white raster display.

[0106] FIG. 7 is a diagram illustrating relations between the display gradation and the power consumption during the white raster display. In FIG. 7, the horizontal axis represents the display gradation and the vertical axis represents the power consumption during the white raster display. The dashed line drawn in FIG. 7 represents a power consumption Wall during the white raster display. The solid line drawn in FIG. 7 represents a first power Wadd obtained by summing a power Wr, a power Wg, and a power Wb required for displaying single-color rasters (R raster, G raster, and B raster) having the same gradation as the display gradation in the white raster display, as given by Expression (5) below. The long dashed short dashed line drawn in FIG. 7 represents a second power We serving as a power consumption value calculated on the preliminary assumption that the actual power consumption decreases therefrom. FIG. 7 illustrates an example in which the display is performed at a maximum of 255 gradation levels.

$$W_{add} = W_r + W_g + W_b \quad (5)$$

[0107] As illustrated in FIG. 7, the ratio (Wall/Wadd) between the power consumption Wall during the white raster display and the first power Wadd obtained by summing the power Wr, the power Wg, and the power Wb required for displaying the single-color rasters having the same gradation as the display gradation in the white raster display is proportional at each of the gradation levels. In other words, a ratio (Wallmax/Waddmax) between a maximum power consumption value Wallmax during the white raster display at the maximum gradation level and a maximum total power consumption value Waddmax obtained by summing a maximum power value Wrmax of the power Wr, a maximum power value Wgmax of the power Wg, and a maximum power value Wbmax of the power Wb required for displaying the single-color rasters having the same gradation as the display gradation in the white raster display at the maximum

gradation level is applied as a constant value to all the gradation levels. In this case, the power consumption value W_{all} during the white raster display is represented by Expression (6) below.

$$W_{all}=W_{add}\times(W_{allmax}/W_{addmax}) \quad (6)$$

[0108] That is, Expression (7) below represents a difference between the power consumption W_{all} during the white raster display and the first power W_{add} obtained by summing the power W_r , the power W_g , and the power W_b required for displaying the single-color rasters having the same gradation as the display gradation in the white raster display.

$$\begin{aligned} W_c &= W_{add} + (W_{add} - W_{add} \times (W_{allmax}/W_{addmax})) \\ &= W_{add} \times (1 + (1 - (W_{allmax}/W_{addmax}))) \end{aligned} \quad (8)$$

[0109] That is, to make the actual power consumption substantially equal to the first power W_{add} obtained by summing the power W_r , the power W_g , and the power W_b required for displaying the single-color rasters having the same gradation as the display gradation in the white raster display, a value corresponding to the difference represented by Expression (7) needs to be added to the value of the video signal to be supplied to the organic EL panel 10. That is, the video signal needs to be controlled such that Expression (8) below gives the second power W_c serving as the power consumption calculated on the preliminary assumption that the actual power consumption decreases therefrom, as illustrated by the long dashed short dashed line in FIG. 7.

$$\begin{aligned} W_{add} - W_{all} &= W_{add} - W_{add} \times (W_{allmax}/W_{addmax}) \\ &= W_{add} \times (1 - (W_{allmax}/W_{addmax})) \end{aligned} \quad (7)$$

[0110] In the present embodiment, Expression (8) given above is deformed into Expression (9) below. That is, the first power W_{add} obtained by summing the power W_r , the power W_g , and the power W_b required for displaying the single-color rasters having the same gradation as the display gradation in the white raster display is multiplied by a coefficient α to obtain the second power W_c serving as the power consumption calculated on the preliminary assumption that the actual power consumption decreases therefrom.

$$W_c=W_{add}\times\alpha \quad (9)$$

[0111] (where $\alpha=1+(1-(W_{allmax}/W_{addmax}))$)

[0112] When W_t denotes the maximum allowable power that is allowed when the organic EL panel 10 performs the image display, the luminance adjustment needs to be performed such that the actual power consumption does not exceed the maximum allowable power W_t . In this case, Expression (10) below represents a threshold power W_{th} .

$$W_{th}=W_t\times\alpha \quad (10)$$

[0113] In a region where the second power W_c exceeds the threshold power W_{th} , the power consumption can be reduced to the threshold power W_{th} or smaller by multiplying the second power W_c by a luminance adjustment gain G represented by Expression (11) below.

$$G=W_{th}/W_c \quad (11)$$

[0114] FIG. 8 is a diagram illustrating an exemplary result of the luminance adjustment in the case of the white raster display in the display device according to the embodiment. In FIG. 8, the horizontal axis represents the display gradation and the vertical axis represents the power consumption during the white raster display.

[0115] FIG. 8 illustrates an example in which the second power W_c is equal to the threshold power W_{th} in a region where the gradation level is equal to or higher than N . According to this example, the actual power consumption is limited to or below the maximum allowable power W_t that is allowed when the organic EL panel 10 performs the image display.

[0116] While the above has described the specific example of the luminance adjustment during the white raster display, the same applies in the case where the complementary color raster display is performed, and in the case where a natural image is displayed. That is, in the display operation of the received video signal, the second power W_c is obtained by multiplying the first power W_{add} serving as the total value of the power W_r required for displaying red (first color), the power W_g required for displaying green (second color), and the power W_b required for displaying blue (third color) by a predetermined coefficient according to the video signal.

[0117] The following describes specific examples of the coefficient α .

[0118] For example, in the single-color raster display of red (R), green (G), and blue (B), Expressions (12), (13), and (14) given below hold. In other words, the coefficient is given as $\alpha_1=1$ in the single-color raster display.

$$W_{all}=W_r \quad (12)$$

$$W_{all}=W_g \quad (13)$$

$$W_{all}=W_b \quad (14)$$

[0119] For example, in the complementary color raster display of yellow (Y), magenta (M), and cyan (C), the coefficient is denoted as α_2 , and is equal among these colors.

[0120] For example, in the white raster display, the coefficient is denoted as α_3 .

[0121] When the natural image is displayed, the coefficient α can have any value. In the present embodiment, the following describes an example in which a plurality of types of patterns are set in advance, and coefficients α_4-1 , α_4-2 , α_4-3 , . . . , α_4-p (where p is a natural number) are set according to each of the patterns. The present disclosure is not limited by the method of setting or method of distinguishing the patterns. The method of determining the coefficient α is not limited to that described above, and the present disclosure is not limited by the method of determining the coefficient α .

[0122] The following describes a specific configuration for performing the above-described luminance adjustment according to the present embodiment. FIG. 9 is a diagram illustrating an exemplary circuit block configuration for performing the luminance adjustment according to the embodiment.

[0123] As illustrated in FIG. 9, the image processor 111 of the controller 11 includes an image analyzer 113 and a luminance adjuster 114. The present embodiment is configured to perform the luminance adjustment on the video signal V_{disp} after being subjected to the gamma conversion.

[0124] The controller 11 includes a storage unit 115 that stores in advance various parameters to be used in the luminance adjustment by the image processor 111.

[0125] FIG. 10 is a diagram illustrating an example of coefficient information including the coefficients for the respective patterns of the video signal. FIG. 10 illustrates the example, as coefficient information D1, in which a coefficient when the video signal is a signal to display a red raster (single-color raster (R)), a coefficient when the video signal is a signal to display a green raster (single-color raster (G)), and a coefficient when the video signal is a signal to display a blue raster (single-color raster (B)) are stored each as the coefficient $\alpha 1$ (=1) in the storage unit 115; a coefficient when the video signal is a signal to display a yellow raster (complementary color raster (Y)), a coefficient when the video signal is a signal to display a magenta raster (complementary color raster (M)), and a coefficient when the video signal is a signal to display a cyan raster (complementary color raster (C)) are stored each as the coefficient $\alpha 2$ in the storage unit 115; a coefficient when the video signal is a signal to display a white raster (white raster (W)) is stored as the coefficient $\alpha 3$ in the storage unit 115; and coefficients when the video signals are signals to display natural images (natural image (pattern 1), natural image (pattern 2), natural image (pattern 3), . . . , natural image (pattern p)) of patterns 1, 2, 3, . . . , p (where p is a natural number) are stored as the coefficients $\alpha 4-1$, $\alpha 4-2$, $\alpha 4-3$, . . . , $\alpha 4-p$, respectively, in the storage unit 115. Each of the coefficients may be numerical data, or may be a discrete value, such as digital data.

[0126] FIG. 11 is a diagram illustrating an example of maximum power information including the maximum power values for the respective colors each required for displaying the single-color raster at the maximum gradation level. FIG. 11 illustrates the example, as maximum power information D2, in which the maximum power value W_{rmax} required for displaying the single-color raster (R) at the maximum gradation level, the maximum power value W_{gmax} required for displaying the single-color raster (G) at the maximum gradation level, and the maximum power value W_{bmax} required for displaying the single-color raster (B) at the maximum gradation level are stored in the storage unit 115. Each of the maximum power values may be numerical data, or may be a discrete value, such as digital data.

[0127] FIG. 12 is a flowchart illustrating an exemplary luminance adjustment procedure according to the embodiment. The following describes an operation of the image processor 111 according to the flowchart illustrated in FIG. 12.

[0128] The image analyzer 113 first analyzes a received video signal VDISP for one frame (Step S101). Examples of methods of image analysis in the image analyzer 113 include a histogram analysis. The present disclosure is, however, not limited by the method of image analysis in the image analyzer 113.

[0129] Based on the result of the image analysis, the image analyzer 113 reads a coefficient according to the video signal VDISP from the storage unit 115 (Step S102).

[0130] For example, if the video signal VDISP is a signal indicating to display the single-color raster (R), the single-color raster (G), or the single-color raster (B), the image analyzer 113 reads the coefficient $\alpha 1$ (=1) from the storage unit 115.

[0131] For example, if the video signal VDISP is a signal indicating to display the complementary color raster (Y), the complementary color raster (M), or the complementary color raster (C), the image analyzer 113 reads the coefficient $\alpha 2$ from the storage unit 115.

[0132] For example, if the video signal VDISP is a signal indicating to display the white raster (W), the image analyzer 113 reads the coefficient $\alpha 3$ from the storage unit 115.

[0133] For example, if the video signal VDISP is a signal indicating to display a natural image, the image analyzer 113 determines which of the patterns 1, 2, 3, . . . , p is the most similar to the video signal VDISP, and reads an appropriate one of the coefficients $\alpha 4-1$, $\alpha 4-2$, $\alpha 4-3$, . . . , $\alpha 4-p$ according to the most similar one of the patterns 1, 2, 3, . . . , p.

[0134] The image analyzer 113 subsequently extracts the red (R) component, the green (G) component, and the blue (B) component included in the video signal VDISP (Step S103). The image analyzer 113 reads the maximum power values W_{rmax} , W_{gmax} , and W_{bmax} from the storage unit 115, and obtains the power W_r required for displaying the red (R) component, the power W_g required for displaying the green (G) component, and the power W_b required for displaying the blue (B) component (Step S104).

[0135] The image analyzer 113 calculates the first power W_{add} serving as the total of the power W_r , the power W_g , and the power W_b (Step S105). The image analyzer 113 multiplies the calculated first power W_{add} by the coefficient read from the storage unit 115 at Step S102 to obtain the second power W_c , and multiplies the maximum allowable power W_t that is allowed when the organic EL panel 10 performs the image display by the coefficient read from the storage unit 115 at Step S102 to obtain the threshold power W_{th} (Step S106). The image analyzer 113 outputs the second power W_c , the threshold power W_{th} , and the coefficient to the luminance adjuster 114.

[0136] The luminance adjuster 114 includes a frame buffer that holds the video signal VDISP for one frame while the image analyzer 113 performs the processing from Step S101 to Step S106 described above.

[0137] The luminance adjuster 114 determines whether the second power W_c received from the image analyzer 113 is equal to or greater than the threshold power W_{th} (Step S107).

[0138] If the second power W_c received from the image analyzer 113 is less than the threshold power W_{th} (No at Step S107), the luminance adjuster 114 outputs the video signal V_{disp} obtained by multiplying the video signal VDISP for one frame by the coefficient (Step S108).

[0139] If the second power W_c received from the image analyzer 113 is equal to or greater than the threshold power W_{th} (Yes at Step S107), the luminance adjuster 114 outputs the video signal V_{disp} that is obtained by multiplying the video signal VDISP for one frame by the coefficient and further multiplying the result by the ratio (W_{th}/W_c) between the threshold power W_{th} and the second power W_c as the gain G (Step S109).

[0140] The processing described above is performed for each frame, and thus, the luminance adjustment can be appropriately performed regardless of the video signal.

[0141] In the present embodiment, the example has been illustrated in which the coefficient $\alpha 1$ has the common value of 1 when the single-color raster (R, G, or B) is displayed. The coefficients may, however, be different from one another when the single-color raster (R), the single-color raster (G),

or the single-color raster (B) is displayed. The example has also been illustrated in which the coefficient α_2 is common when the complementary color raster (Y, M, or C) is displayed. The coefficients may, however, be different from one another when the complementary color raster (Y), the complementary color raster (M), or the complementary color raster (C) is displayed.

[0142] As described above, the display device **1** according to the embodiment includes: the organic EL panel **10**, or μ LED panel, that includes a plurality of first light-emitting elements for emitting red (first color), a plurality of second light-emitting elements for emitting green (second color), and a plurality of third light-emitting elements for emitting blue (third color); the image analyzer **113** that obtains, in the display operation of the received video signal VDISP, the first power W_{add} serving as the total of the power W_r required for displaying red (first color), the power W_g required for displaying green (second color), and the power W_b required for displaying blue (third color), and that calculates the second power W_c by multiplying the first power W_{add} by the predetermined coefficient according to the video signal DISP and calculates the threshold power W_{th} by multiplying, by the coefficient, the maximum allowable power W_t that is allowed when the organic EL panel **10** performs the image display; and the luminance adjuster **114** that multiplies the video signal VDISP by the ratio between the threshold power W_{th} and the second power W_c when the second power W_c is equal to or greater than the threshold power W_{th} .

[0143] With this configuration, the actual power consumption in the organic EL panel **10** can be reduced to or below the maximum allowable power W_t .

[0144] The luminance adjuster **114** can prevent the luminance from decreasing in a low-luminance region where the power consumption is equal to or lower than the maximum allowable power W_t by multiplying the video signal VDISP by the coefficient, regardless of the level of the second power W_c .

[0145] Specifically, the image analyzer **113** employs the coefficient α_3 (first coefficient) if the video signal VDISP is the signal indicating to display the white raster, and employs the coefficient α_1 (second coefficient) if the video signal VDISP is the signal indicating to display the single-color raster.

[0146] If the video signal VDISP is the signal indicating to display the single-color raster, the image analyzer **113** varies the coefficient α_1 (second coefficient) according to the color of the single-color raster.

[0147] The image analyzer **113** employs the coefficient α_2 (third coefficient) if the video signal VDISP is the signal indicating to display the complementary color raster.

[0148] If the video signal VDISP is the signal indicating to display the complementary color raster, the image analyzer **113** varies the coefficient α_2 (third coefficient) according to the color of the complementary color raster.

[0149] The image analyzer **113** employs one of the coefficients α_4-1 , α_4-2 , α_4-3 , . . . , α_4-p (fourth coefficient) if the video signal VDISP is the signal indicating to display the natural image. If the video signal VDISP is the signal indicating to display the natural image, the image analyzer **113** employs different one of the coefficients α_4-1 , α_4-2 , α_4-3 , . . . , α_4-p (fourth coefficient) according to corresponding one of the patterns 1, 2, 3, . . . , p of the natural image.

[0150] According to the present embodiment, the display device **1** can be provided that can appropriately adjust the luminance regardless of the video signal.

[0151] The components of the embodiment described above can be combined as appropriate. Other operational effects accruing from the aspects described in the present embodiment that are obvious from the description herein, or that are appropriately conceivable by those skilled in the art will naturally be understood as accruing from the present disclosure.

What is claimed is:

1. A display device comprising:

an electroluminescent (EL) panel comprising a plurality of first light-emitting elements configured to emit a first color, a plurality of second light-emitting elements configured to emit a second color, and a plurality of third light-emitting elements configured to emit a third color;

an image analyzer configured to obtain, in displaying of a received video signal, a first power serving as a total value of a power required for displaying the first color, a power required for displaying the second color, and a power required for displaying the third color, and configured to calculate a second power by multiplying the first power by a predetermined coefficient according to the video signal, and calculate a threshold power by multiplying, by the coefficient, a maximum allowable power that is allowed when the EL panel performs image display; and

a luminance adjuster configured to multiply the video signal by a ratio between the threshold power and the second power when the second power is equal to or greater than the threshold power.

2. The display device according to claim 1, wherein the luminance adjuster is configured to multiply the video signal by the coefficient regardless of the level of the second power.

3. The display device according to claim 1, wherein the image analyzer is configured to set the coefficient to a first coefficient when the video signal is a signal indicating to display a white raster, and to set the coefficient to a second coefficient different from the first coefficient when the video signal is a signal indicating to display a single-color raster.

4. The display device according to claim 3, wherein the image analyzer is configured to vary the second coefficient according to a color of the single-color raster when the video signal is the signal indicating to display the single-color raster.

5. The display device according to claim 1, wherein the image analyzer is configured to set the coefficient to a third coefficient different from the first coefficient and the second coefficient when the video signal is a signal indicating to display a complementary color raster.

6. The display device according to claim 5, wherein the image analyzer is configured to vary the third coefficient according to a color of the complementary color raster when the video signal is the signal indicating to display the complementary color raster.

7. The display device according to claim 1, wherein the image analyzer is configured to set the coefficient to a fourth coefficient different from the first coefficient, the second coefficient, and the third coefficient when the video signal is a signal indicating to display a natural image.

8. The display device according to claim 7, wherein the image analyzer is configured to vary the fourth coefficient according to a pattern of the natural image when the video signal is the signal indicating to display the natural image.

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[标]申请(专利权)人(译)	株式会社日本显示器		
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摘要(译)

一种显示装置，包括：电致发光面板，包括发射红色的第一发光元件（第一颜色）；发射绿色的第二发光元件（第二颜色）；以及发射蓝色的第三发光元件（第三颜色）；一种图像分析仪，在显示接收的视频信号时，获得第一功率，用作显示红色（第一种颜色）所需的功率，显示绿色所需的功率（第二种颜色），以及显示蓝色所需的功率（第三种颜色）通过根据视频信号将第一功率乘以预定系数来计算第二功率，并且通过将系数乘以当电致发光面板执行图像显示时允许的最大允许功率来计算阈值功率；和亮度调节器，当第二功率等于或大于阈值功率时，该亮度调节器将视频信号乘以阈值功率和第二功率之间的比率。

